# DSM reliability: Do we care about?

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**High reliability (hi-rel) users of advanced microelectronic products face many challenges as technology scales into deep sub-micron feature sizes. Because the desire for higher performance, lower operating power, and lower stand-by power characteristics continue to be sought after in hi-rel systems. International Technology Roadmap for Semiconductors (ITRS) predictions over the next few years will drive manufacturers to reach both physical and material limitations as technology continues to scale. As a result, new materials, designs and processes will be employed to keep up with the performance demands of the consumers' industry. These aspects, in addition to higher power and thermal densities, increase the risk of introducing new failure mechanisms and accelerating known failure mechanisms.**

*Keywords: Deep Sub-Micron, Wear-out, Reliability, Physics-of-Failure,*

## 1. Introduction

Both the processing and networking technologies are driven by the consumer market which entirely redefines the way embedded and complex systems are designed in the future. The advantages of this are clear in terms of reduced size, weight and power consumption. However the advent of more sophisticated embedded systems that support more powerful functions, and the reliance on DSM process technologies for their fabrication, have brought reliability concerns to the forefront ([1] [2]). For most of products, these inconveniences are not an issue, reliability requirements are still achieved (only 1 to 5 years operational lifetime target and up to a failure rate of 1000 FITs). But in avionic domain, reliability is a major issue because lifetime requirements are much higher (over 25 years lifetime target and a maximum failure rate of 100 FITs), in harsh operational conditions.

## 2. Technology evolution and critical issues for devices miniaturization

### 2.1 Technology evolution : from history to present

Electronic device performances have improved dramatically over the decades, enabled by significant advances in integrated circuit (IC) technology evolution. In 1965, Gordon E. Moore the co-founder of Intel sketched out his prediction of the pace of silicon technology [3]: the number of components in integrated circuits had doubled every year from the invention of the IC in 1958 until 1965. He predicted that the trend would continue "for at least ten years". After that, Moore slightly altered the formulation of the law over time, in 1975. He altered it to a doubling every two years. His prediction has been proved to be uncannily accurate in recent technology evolution and will continues, in part because this law is now used in the semiconductor industry to guide long term planning and to set targets for research and development, depicted in Figure 1.

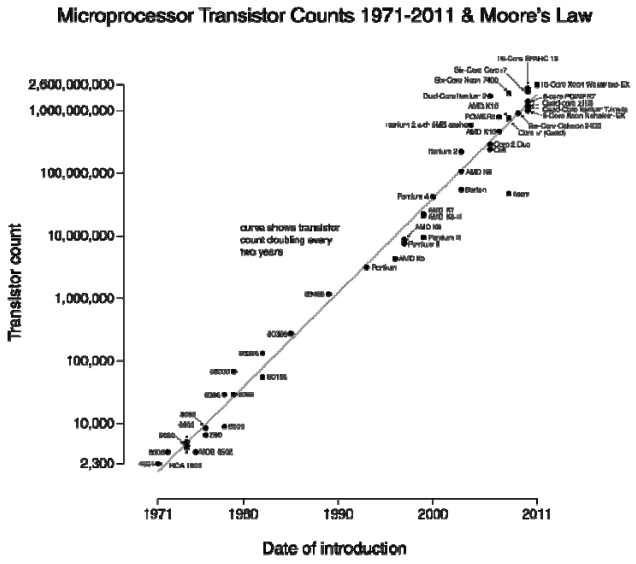


**Figure 1. CPU transistor counts against dates of introduction;**

While Moore's Law only describes the rate of increase in transistor density, reduction of the physical MOS device dimensions has improved both circuit speed and density. Technology scaling is the critical parameter of transistor roughly scaled by a factor k ($k \approx 0.7$) in every generation (2 years). In 1974, Dennard proposed a scaling rule: constant field scaling [4], all device dimension are scaled by the same factor "k" and the supply voltage and other voltage (as threshold voltage) are also same scaled to maintain a constant electric field throughout the device.

The original form scaling could reduce the gate delay and hold the power density constant. But for the reason of compatibility of power supply in the system design, the supply voltage needs to be consistent with the system specification. Constant field scaling was replaced with constant voltage scaling at 1980, and instead of remaining constant , the electric fields inside the device increased from generation to generation until the early 1990s, when excessive power dissipation and heating, some reliability degradations caused serious problems with the stronger electric field.

### 2.2 Limitations of technology scaling and critical issues for circuit reliability

Due to the atomic limits, the key parameter as gate length could not scale indefinitely. Alternate process technology has been developed to continue the Moore's law. The gate oxides have been shrinking in thickness right along with the gate length shrinks. With the gate length shorter than 90nm, the gate thickness is reaching to 2nm which only representing 6 to 7 atomic layers of silicon dioxide (SiO2). SiO2 is less and less as a good insulator and electrical leakage will become serious until unacceptable, which could increase the static power consumption of the circuit. In practice, the scaling variables don't scale in the same way. Figure 2 shows the trends of power supply voltage, threshold voltage, and gate oxide thickness versus channel length for high performance CMOS technologies [5].

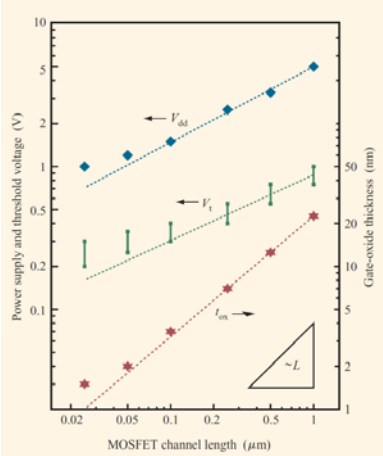


**Figure 2. History and trends of power supply voltage (Vdd), threshold voltage (Vth) vs. channel length for CMOS logic technologies.**

With the scaling theory, threshold voltage (Vth) should scale at the same rate as the other device, however, with the consideration of static power consumption, Vth could not be reduced with the same trend. Sub-threshold current which dominates the total leakage current varies exponentially with Vth. Power supply voltage has to keep a gap with Vth to maintain a reasonable gate over drive. That is why that the power supply voltage has not been decreased at a linear rate to the channel length and oxide thickness. It means that the electric field has been gradually rised over the generations. The asymmetrical scale between power supply and device dimensions can also increase the power density of the chip, consequently raising the junction temperature. This could accelerate the degradation of circuit reliability.

## 3. IC reliability issues in Deep Sub-Micron Technologies

### 3.1 IC reliability concerns

A central cause of the failure of systems built with integrated circuits is the aging of transistors that make up the digital and analog circuits. The challenge of predicting the reliability of electronic systems is to predict the changing characteristics of the components these systems are built on, the transistors. The reliability of ICs is always the critical problem which had to be dealt with. These new technologies become far less mature than earlier ones, e.g. introduction of new materials and process steps that

are not fully characterized leading to potentially less reliable products. Indeed, DSM technologies come with issues that need solutions. Among others, they include new variability and reliability effects that are intrinsic to technology scaling and will impact the "well know" bath curve as shown in figure 3.

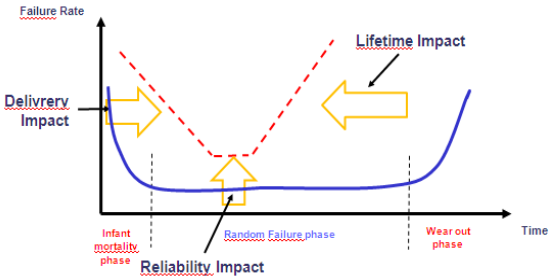


**Figure 3: DSM impact on the bath curve**

During their useful life, ICs are affected by different degradation mechanisms, such as hot carrier injection (HCI), negative bias temperature instability (NBTI), time-dependent dielectric breakdown (TDDB), which are illustrated in Figure 4. These degradation mechanisms can shift the properties of electronic devices and thereby affect the circuit performance. Furthermore the degradation mechanisms can be accelerated by harsh operation conditions (high/low temperature, electrical overstress, and radiation) which reduce the device lifetime

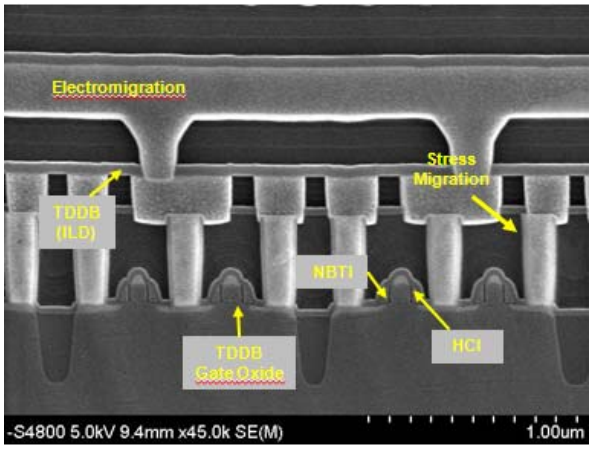


**Figure 4 :Wear-out phenomena localization (65 nm IC cross section)**

- Time Dependent Dielectric-Breakdowns (TDDB) mainly in gate oxide of devices (especially dramatic in hig-K oxides) but also on inter-level Dielectrics,
- Negative Bias Temperature Instability (NBTI) is a phenomenon that causes a drift of the threshold voltage of CMOS transistors,
- Electro-Migration (EM) failure mechanism experienced by interconnect
- Hot carrier injection (HCI) occurs when carriers gain sufficient energy to be injected into the gate oxide. Defects can be created at the oxide interface or within the oxide. This mechanism results in the degradation of drive currents, and the decrease of switching frequency.

- Stress migration (SM) which come from the mismatch of the thermal expansion Coefficient of the different layers of the die and may induce the formation of voiding in interconnects. The risk increases with technology scaling

Those mechanisms were considered as second-order effects in the past and become a clear threat for the parametric and functional operation of the circuits and systems today as they all result in drastic change in the device electrical characteristics and bring a shrink of the bathcurve. The time to wear-out or the lifetime of the device depends not only on the IC technology, but also on environment, as temperature, supply voltage, the operating frequency or clock duty cycle. All of them could accelerate the failure mechanism and reduce the device lifetime.

The traditional statistical reliability analysis approach consist of determine the MTBF or FIT which is a simple statistic model based on measurement and without the relation with failure mechanism. There are several limitations of this approach. First, in the real condition, the wear out step consists of different degradation mechanisms instead of single failure. Additional, with the technology evolution, the lifetime of the device would be much lower, as this statistical model is accurate of the device operate over decades, however for the device lifetime less than several year, the model could be not accurate enough. Furthermore, enter the submicron technology, the soft failure (degradation failure) are the main failures instead of catastrophic failures which the device are totally destroyed. How to predict the system performance degradation due to the device parameter variation?

### 3.2 The physics of failure approach

To overcome the limitation of traditional approach, recently reliability researches proposed Physics of failure (PoF) approach [6] which identify the failure during design level as opposed to a traditional which analysis after failure are observed during qualification tests. It is based on separate study of the dominant failure mechanisms: their root causes, the failure modes and failures causing stresses. The procedure of physic of failure approach consists by firstly identifying the dominant failure mechanisms, then, creating the PoF models by combination the data gathered from acceleration test and statistical distributions. And in the end develop an equation for the failure mechanism for simulation and prognostics.

#### 3.2.1 Electromigration (EM)

With high current densities, the electron can transfer sufficient momentum to thermally activate metal atoms, forcing them break the electrostatic force and escape out of their lattice sites, then extracted atoms move under diffusion in the same direction as electron.

In an ideal conductor, where atoms are arranged in a perfect lattice structure, electrical resistance is Zero, i.e. electrons moving through the conductor would experience no collisions. In a real conductor, defects in the lattice structure, as missing atoms (vacancies), impurities...and the random thermal vibrations of the metal atoms out of their positions cause electrons to collide with the atoms and scatter. The scattering event makes the electron change direction and also acceleration. In the other side, the electrostatic force in symmetric and uniform lattice has a resistance to collisions. But the metal atoms in an imperfect lattice with

vacancies, grain boundaries and material interface, have weak bonds and could be easier pushed away from their position, and transported in the current direction. The direction is also influenced by grain boundaries itself, as atoms are transported along the direction of the boundaries.

As device features continue to shrink, the thinner film brings fine grain size whose Ea become lower. The interconnect current densities growing, joule heating causes temperature increasing. The increased performance require that interconnects have to be more and more reliable under conditions where metallization is inherently less reliable [7].

#### 3.2.2 Hot Carrier Injection (HCI)

Hot carrier injection is one of the primary wear out failure mechanism affecting the long term reliability of ICs. It has been aggravated due to continuous scaling of MOS transistor dimensions without proportional scaling of the operation voltage, which causes a significant increase of the gate electric field in both horizontal and vertical direction, The carriers (electrons or holes) under these high electric fields gain enough kinetic energy which exceeds the average energy lost by the carrier through the scattering effects. The effective carrier temperature will be larger than the lattice temperature. Such a carrier is termed as "hot carrier" [8]. These hot carriers could be injected into the gate oxide, causing permanent changes to the charge distribution at the oxide-interface. It would induce device degradation as threshold voltage (*Vt*) shift and reduction of drain current.

HCI effects are enhanced at low temperature as its activation energy is negative (around -1eV), mainly explained by the increase of electron mean free path and impact ionization rate rising at low temperature. The research results show that substrate current at 77K is five times greater than that at room temperature (RT). At low temperature, the electron trapping efficiency increases and the effect of fixed charges becomes large. This accelerates the degradation of transconductance (Gm) at low temperature.

Other environmental condition like the radiation exposure (X- ray, gamma ray, solar proton…) can increase HCI degradation rate, as total dose damage, the produced damages have almost the same mechanism as the hot carrier injection [9].

#### 3.2.3 Time Depend Dielectric Breakdown (TDDB)

The TDDB failure mechanism takes place in three stages: the first stage is built up stage which last over a long period of time. The gate oxide is slowly damaged and degraded due to the localized hole and bulk electron trapping inside the oxide and in the Si/SiO2 interface. The second stage begins when the increasing density of traps form a resistive conduction path (called percolation path) through the oxide and the localized high field/current density inside oxide reach a critical value.

With the technology scaling, the transistor oxide thickness continue to shrink to below 2nm. As **Erreur ! Source du renvoi introuvable.** in fig 5, after the first step, the percolation path is created and transistors begin to suffer soft breakdown failure with gate leakage current slowly increasing. But the circuit could always function without failure [10].

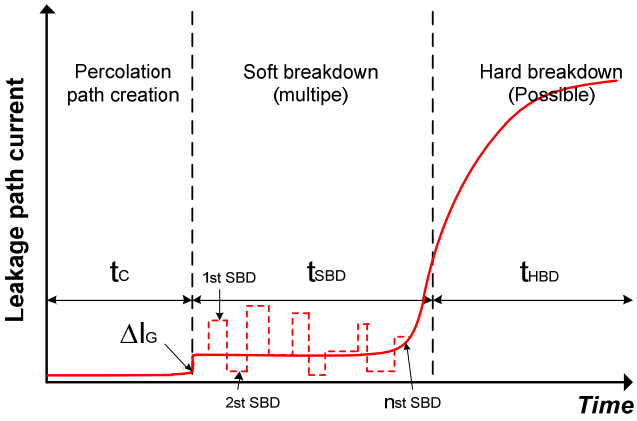


**Figure 5 : Three stages of breakdown in thin oxide transistor.**

But in the second stage, transistor could be suffered multiple SBD, and the cumulative failure could reach 20% variation of threshold voltage. When the gate leakage reaches a critical threshold, the breakdown evolves into the third stage: HDB which has a catastrophe level of leakage current through the oxide.

### 3.2.4 BIAS Temperature Instability (BIT)

The bias temperature instability (BTI) is a degradation problem for MOSFETs, which has been studied since the 1960s. In the recent year, it became a widely concern issue in IC reliability, since the gate electric fields have increased with transistor dimension scaling, chip operating temperature increase, replacement of buried channel MOSFET by surface channel. In the BTI issue, the most important and interesting issue is the Negative bias temperature instability (NBTI) for PMOS. Under the negative bias and elevated temperature, there are interface traps and oxide charge created inside the oxide of PMOS. The NBTI phenomena could degrade transistor performance by increasing the absolute threshold voltage, decreasing the mobility, transconductance, drain current. (Figure 6)

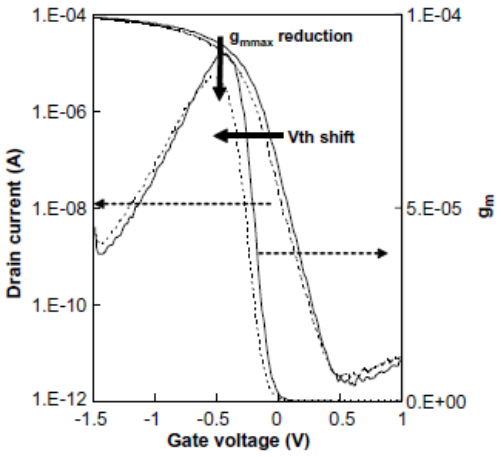


**Figure 6 : Id – VG and Gm – VG curve for fresh device (full line) and after 10,000 s of stress (dashed line) for a PMOS with 2nm thick oxide at 125°C in the linear regime**

Degradations due to NBTI tend to recover after the stress removed. The mechanism of recovery is always an open question for researchers. Huard at al.have done extensive measurements and find partial recover [11]. They attribute NBTI

degradation due to interface trap generation and hole trapping. When the stress on gate removed or change to positive voltage could reduce the degradation of the device, as the X species might move back from the oxide to interface forming the repassivation of the Si dangling bonds and the holes trapping in oxide could be neutralized. The experiments made by Huard [11] showed that the interface trap density remains largely unchanged during the recovery phase. The recovery of NBTI degradation mainly due to the hole trapping relaxed during recovery, the positive voltage could neutralize the trapped holes.

In the previous paragraphs, we introduced four important degradation mechanisms: Electromigration (EM), Hot carrier injection (HCI), Time dependent dielectric breakdown (TDDB), and Negative bias temperature instability (NBTI). In the wear-out phase, they could degrade interconnection and gate oxide integrity. And thereby induce circuit functionality failure.

### 3.3 DSM Reliability Studies

Reliability has been defined as:

*The probability that an item perform a required function under stated conditions for a stated period of time;*

For an IC, their period operation time (lifetime) always depends on the variety application. To avoid IC to be the bottleneck of the whole system reliability, the IC manufacturer should pay attention to address the IC reliability issues. Although in the electronics product customer point of view, the cost is the most important factor in IC design and manufactory, electronic product manufacturers should be only guaranteed several years' proper operation. Systems where reliability is a critical issue, as automotive, aeronautic systems, a nuclear plant…the reliability of ICs is always the critical problem which had to be dealt with.

There are two important types of failure for semiconductor device:

- Degradation failures (soft failure): when an important parameter (as the saturation current or threshold voltage) of the component drift so far from its original value that exceed some specific limit.
- Catastrophic failures (hard failure): the sudden and complete failure of the device, recovery not possible, the end of the device.

Electronic component Reliability is well described by a bathtub shape curve representing the variation of failure rate over time. (was initially developed to model the failure rate of mechanical equipment. However, it has been adapted by the semiconductor industry to model IC failure [12]).

The bathtub curve does not depict the failure rate of a single item, but describes the relative failure rate of an entire population of device over time. It consists of three regions:

- Infant mortality: in this region, Due to manufacturing defects, there are components that fail at relatively higher rate over a short period of time and this part of bathtub curve is known as infant mortality.

- Usefull life,: in this region, the failure rate is relatively constant, during a period dependent on the technology of the integrated at this stage circuit. failures are catalectic
- Wear out: after the normal life period, the device begins to fatigue and some wear-out failure mechanisms become obviously and with an increasing failure rate. The duration could last for years

Classical technologies (e.g. L > 250 nm) usually have hundred years of useful life so they easily fit with the mandatory lifetime. Components used in high reliability applications belonging to infant mortality part are screened by burn-in therefore these integrated circuits have their reliability mostly related to constant failure rate. Recent DSM reliability studies [13] show that the assumption of a constant failure rate during the product service life cannot be maintained as illustrated by the following figure :

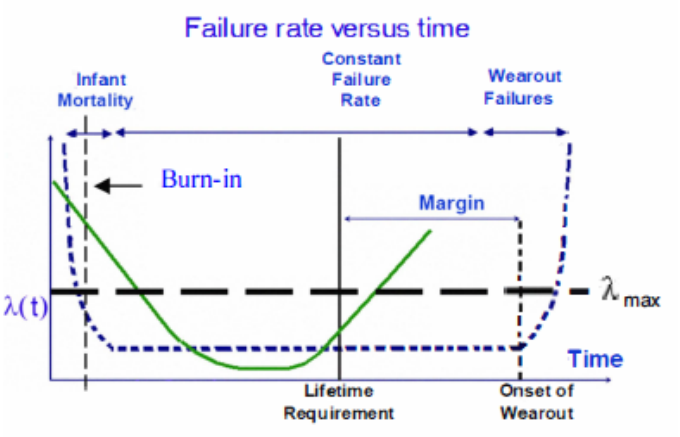


**Figure 7 : Bathtub curve for DSM component [30]**

This result reappraises about safety and maintenance estimations which are performed under a constant failure rate assumption. Usually, wear-out failure mechanisms are modelled by Weibull distribution. Bernstein study [14] gives more precise information and postulates a trend on both scale and shape parameter of the Weibull distribution as illustrated on the following figure :

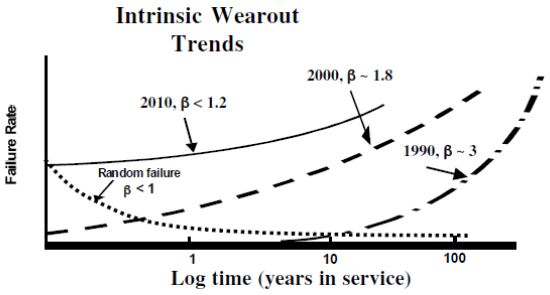


**Figure 8 : Effect of scaling on bathtub curve for DSM component**

We can see that both Weibull parameters decrease as the transistor scaling in DSM decrease. **The question is " what can explain such a behaviour ?"**

3.3.1 Weibull distribution review

For the scale parameter of the Weibull distribution, the physic of failures induced by scale effect described previously explain the decrease of the scale parameter. The exponential distribution usually used to model catalectic failures is a special case of the Weibull distribution where the shape parameter is equal to 1. Each wear-out failure mechanism is characterized by a given shape parameter depending of the its kinetic. The quicker the kinetic is, the greater the shape parameter is.

3.3.2 Dispersion of failures in DSM component

For very law scale, there is a great variability during the manufacturing processes of DSM component. This variability is due to variability in transistor grille length, doping concentration, thickness and height in interconnections …A recent study shows that DSM failures appear into different localizations as illustrated in a DRAM component on the following figure:

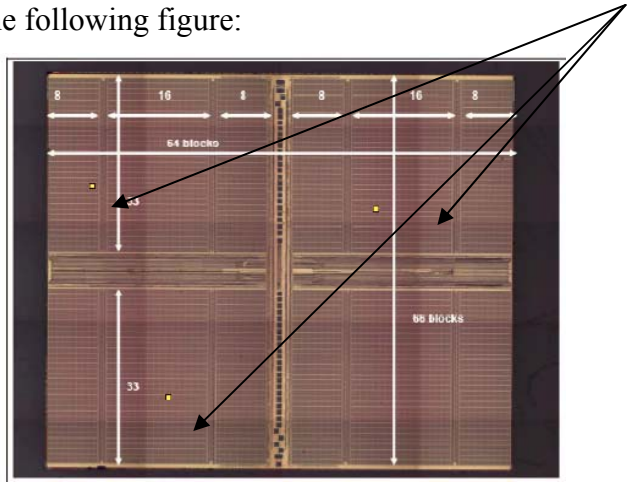


**Figure 9 : Effect of scaling on bathtub curve for DSM component**

At DSM level, failures appear as catalectic failures.

3.3.3 Effect of physical constraint

The survival function of the Weibull distribution is given by eq.1 :

$$S(t) = \exp\left(-\left(\frac{t}{\eta}\right)^{\beta}\right) \quad \text{.....(1)}$$

Where η and β are respectively the scale and the shape parameters. I few take into account the effect of physical constraint X, we obtain for a given failure mechanism: eq2.

$$S(t, X) = \exp\left(-\left(\frac{t}{\eta(X)}\right)^{\beta}\right) \quad \text{.....(2)}$$

For example, the DSM steady-state temperature is not homogeneous on the die and classical Arrhenius law used to model the effect of temperature on the scale parameter can be used directly.

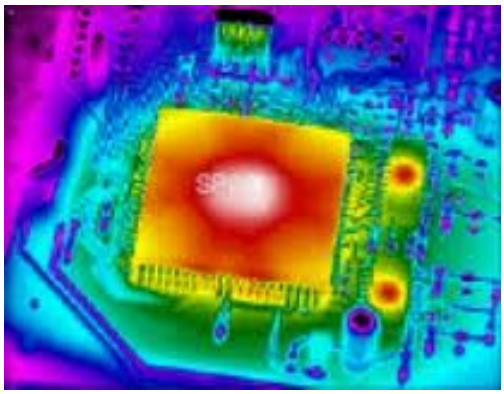

**Figure 9 : temperature distribution for DSM component**

The temperature distribution can be estimate by a given probability density denoted "g" in the physical constraint domain and the survival function can be rewritten as follows (eq.3)

$$S_X(t) = \int_{-\infty}^{+\infty} S(t, X) \cdot g(X) \cdot dX \quad \text{.....(3)}$$

Suppose that the temperature distribution can be estimate by a normal distribution with parameters μ et σ. The survival function is then given by: eq. 4

$$S_X(t) = \int_{-\infty}^{+\infty} \exp\left( -\left( \frac{t}{\eta(X)} \right)^{\beta} \right) \cdot \frac{1}{\sigma \cdot \sqrt{2 \cdot \pi}} \cdot \exp\left[ \frac{-(X-\mu)^2}{2.\sigma^2} \right] \cdot dX \quad \text{.....(4)}$$

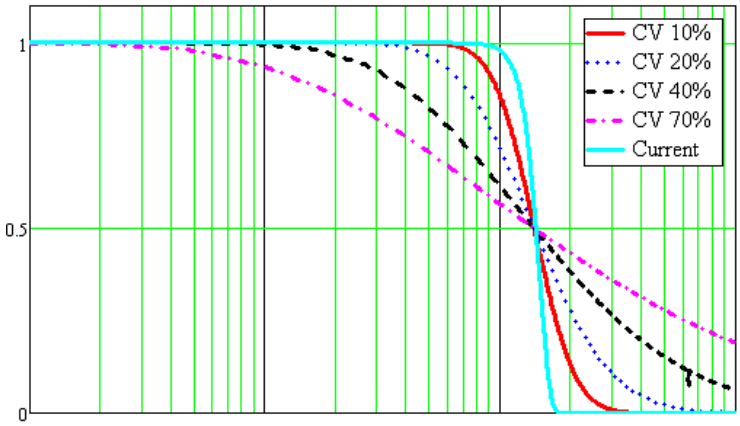


**Figure 10 : Survival function for different DSM temperature distributions**

The previous figure show that the shape parameter trends to decrease as the dispersion of the normal distribution increase (CV coefficient variation).

3.3.4 Maintenance effect

Maintenance policy at the component level is a renewal process because we replace the failed component by a new one. The correct reliability metric for this perfect maintenance is the Rate of Occurrence of Failure denoted by Rocof which is defined by eq.5

$$Rocof(t) = \frac{d}{dt} E[N(t)] \quad \text{.....(5)}$$

where N(t) is the number of failures at time t and E the expected value.
It can be demonstrated that the Rocof is linked to the failure mechanism by its probability density f by:eq.6

$$Rocof(t) = \sum_{i=1}^{+\infty} f^{\langle i \rangle}(t) \quad \text{.....(6)}$$

where $f^{<i>}(t)$ is the "i fold" product convolution.

It can also be proven that $\lim_{t \to +\infty} \text{Rocof}(t) = \frac{1}{MTTF}$

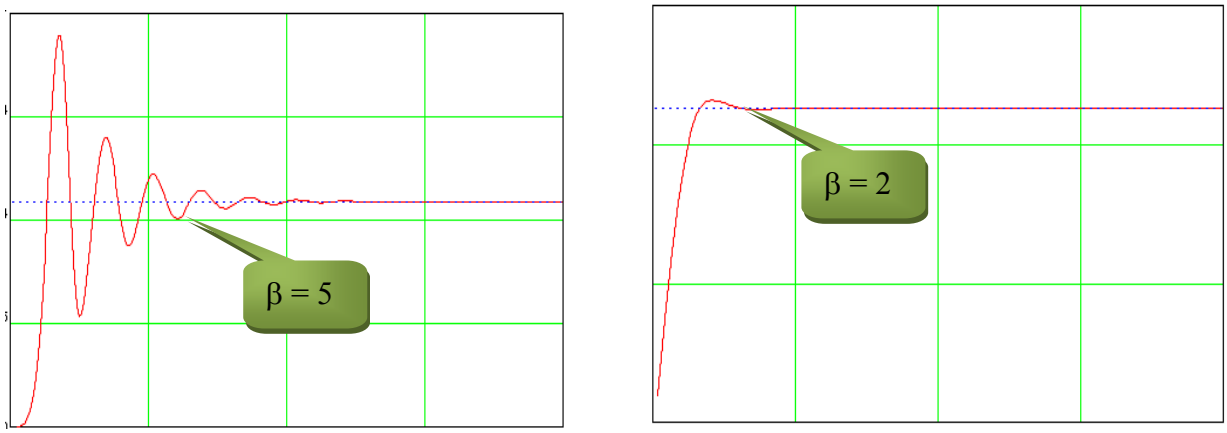


**Figure 11 : Rocof behaviour for different Weibull distribution**

We can note that as the shape parameter trends toward 1, the Rocof converges rapidly to its final value and the approach a constant failure rate.

3.3.5 Effect of the delivery flow

During the entry into service, products which include DSM component have not the same age because products are not delivered at the same time. So, the global Rocof is the superposition of time delayed Rocof which as the effect of smoothing the global Rocof behaviour and approach again a constant failure rate.

## 4. Conclusion

The Moore's law is always checked nowadays and can be correct until 2020, time where DSM technology will have reached the atom physical limit. From Bernstein study, we have proposed different solutions to explain its conclusions from a physical point of view as well as a statistical point of view. Wear-out failure mechanisms, until now considered as neglected, will impact in service reliability of DSM components.

The good news is that quantitative assumptions for Safety and maintenance are always correct even for wear-out failure mechanisms.

The bad news is that the DSM failure rate will be greater than current active component impacting warranty costs, maintenance costs, stock exchange, probability of feared events, …

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